REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove. The Applicants also thank the Examiner for the indication of allowance of Claims 10-17.

Claims 1 - 25 are pending. Of the pending claim set, Claims 1-5 and 7-8 are rejected while Claims 6 and 9 are objected to. Claims 18-25 are withdrawn from consideration. Claim 1 is amended hereinabove.

Claim 1 positively recites implanting a low dose of nitrogen into the semiconductor substrate in a low voltage core region. Claim 1 also positively recites forming an intermediate core gate dielectric layer over an intermediate core region. These advantageously claimed features are not taught or suggested by the publication of Kirkpatrick et al. or the patent granted to Higashitani et al.; either alone or in combination.

The Applicants respectfully traverse the assertion in the Office Action (page 2 that Kirkpatrick et al. discloses "implanting a low dose of nitrogen (332, Fig. 3B) into the semiconductor substrate". The Applicants submit that Kirkpatrick et al. teaches the use of a nitrided dielectric (paragraphs 0010-0011, 0037, 0041) - not a

step of implanting nitrogen into a substrate as advantageously claimed (the Applicants note that nitrogen implantation is completely different than nitridation).

Regarding Claim 4, the Applicants respectfully traverse the assertion in the Office Action (page 3) that Kirkpatrick et al. discloses the thicknesses of the Applicants' gate dielectric layers. The Applicants submit that in paragraph 0027 that Kirkpatrick et al. only discloses a thickness the low voltage gate dielectric. Kirkpatrick et al. does not teach the relative thickness of the intermediate core dielectric layer (which is claimed in Claim 4) because Kirkpatrick et al. does not teach the use of a tri-gate semiconductor device (paragraphs 0009, 0042; see also the content of the first paragraph of page 3 of the Office Action).

Regarding Claim 8, the Applicants respectfully traverse the assertion in the Office Action (page 3) that Kirkpatrick et al. discloses "forming a third gate over the intermediate core dielectric layer [FIG. 4]." The Applicants submit that FIG. 4 only shows a low voltage gate 435 and a high voltage gate 455 (FIG. 4, paragraph 0042). Kirkpatrick et al. does not teach the use of a tri-gate semiconductor device (paragraphs 0009, 0042), as advantageously claimed. More specifically, Kirkpatrick et al. does not teach forming a third gate over the intermediate core dielectric layer as advantageously claimed in Claim 8.

The Applicants respectfully traverse the assertion in the Office Action (page 3) that Higashitani et al. teaches "forming an intermediate core gate dielectric layer (20, Fig. 1) over an intermediate core region layer (18, FIG. 1)." The Applicants submit that element 20 of Higashitani et al. is part of a memory floating gate (column 2 lines 3-4, 7, 14-15, 24, and 43-45), not part of a tri-gate semiconductor device as advantageously claimed. Furthermore, the Applicants submit that element 18 of Higashitani et al. is a memory core (column 1 line 52), not an intermediate core as advantageously claimed.

Moreover, like Kirkpatrick et al., Higashitani et al. does not teach implanting a low does of nitrogen into the semiconductor substrate as advantageously claimed (Claim 1). Therefore, combining the teachings of Kirkpatrick et al. and Higashitani et al. (which is suggested on page 3 of the Office Action) does not teach or suggest the advantageously claimed step of implanting a low does of nitrogen into the semiconductor substrate.

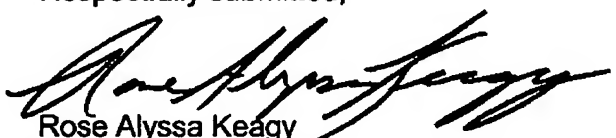
The Applicants respectfully traverse the assertion in the Office Action (page 3) that one of ordinary skill in the art would "modify the above teachings of Kirkpatrick et al. as taught by Higashitani et al. for a purpose of improving a process." The Applicants submit that one of ordinary skill in the art would not combine the teachings of Kirkpatrick et al. and Higashitani et al. because one of ordinary skill in the art would not combine a process that includes plasma

nitridation of the dielectric layer (Kirkpatrick et al., paragraphs 0009-0010) with a process includes thermal oxidation of the dielectric layer (Higashitani et al., column 3 lines 4-14).

Therefore, the Applicants respectfully assert that Claim 1 is patentable over Kirkpatrick et al. and Higashitani et al.; either alone or in combination. Furthermore, Claims 2-9 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the references of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



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